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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,501	03/01/2004	Martin Vorbach	2885/85	1856
26646 7590 02/28/2007 KENYON & KENYON LLP ONE BROADWAY NEW YORK, NY 10004			EXAMINER TRUJILLO, JAMES K	
			ART UNIT 2116	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/28/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/791,501

Applicant(s)

VORBACH ET AL.

Examiner

James K. Trujillo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.138(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 08/946,810.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>112106</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated 12/18/06.
2. Claims 4-19 are presented for examination.

5

Information Disclosure Statement

3. Two references provided in the IDS dated 11/21/06 were not considered because they were considered previously in the IDS dated 3/1/04.

10

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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5. Claims 4-7 and 9 rejected under 35 U.S.C. 102(e) as being anticipated by Durham et al., U.S. Patent 6,785,826.

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6. Regarding claim 4, Durham teaches a data processing device, comprising:
 - a. an array of data processing unit (functional units 206, 210, 214 and 218, figure 2), the processing unit being connected to at least on one of a power supply line and a clock line (system clock 800 via unit clock 804, figure 8; system clock 800 via unit clock 904); and

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b. an enabling/disabling device adapted to at least (low power mode circuits of each functional unit include AND gates 802 figure 8; or MUXes 902, figure 9) to at least one of:

- i. enable or disable power supply to a number of the processing units, and
- 5 ii. block full clock speed for the number of data processing units (the clock is either stopped or reduced for a particular functional unit, col. 7, line 34 through col. 8, line 7);

c. wherein the number is less than all of the processing units (each functional unit controls its own power dissipation, col. 3, lines 44-48); and

10 d. wherein the enabling/disabling devices is configured to be data driven (the enabling/disabling devices are driven by data from the power sensing circuitry, col. 4, lines 45-54);

7. Regarding claim 5, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling device is adapted to
15 provide a clock to a number of the data processing units which is equal to 0 (Durham inherently teaches that clocks all data processing units may be stopped, col. 3, lines 44-48).

8. Regarding claim 6, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling is adapted to be handshake-driven (Durham uses Request lines 208, 214, 220 and 228 along with Status lines
20 210, 216, 222 and 228 to communicate status and requests which are interpreted to be handshake-driven).

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9. Regarding claim 7, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein each of the processing units is a reconfigurable unit of a multi-dimensional array (each functional unit of Durham is reconfigurable because it can change its operating mode, col. 3, lines 44-48).

5 10. Regarding claim 9, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling device is adapted to selectively block full clock speed for the number of data processing units (each functional unit of Durham has clock control, col. 3, lines 44-48, figures 8 and 9).

10 11. Claim 4, 5, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupta et al., U.S. Patent 5,996,083.

12. Regarding claim 4, Gupta teaches a data processing device comprising:

a. an array of data processing units (FU_1 - FU_2 , figure 2), the data processing units being connected to at least one of a power supply line (removing power to functional unit, col. 4, lines 5-7; figure 6 and corresponding text) and a clock line (col. 3, line 67 through col. 4, line 5; figures 3-5 and corresponding text); and

b. an enabling/disabling device adapted (power control 108, figure 2) to at least one of:

i. enable or disable power supply to a number of the processing units (removing power to the functional units, col. 4, lines 5-7), and

ii. block full clock speed for the number of data processing units (col. 3, line 67 through col. 4, line 5);

c. wherein the number is less than all of the processing units (each functional may be provided with it own clock and power control col. 3, lines 47-51; figures 3-6 and corresponding text); and

d. wherein the enabling/disabling devices is configured to be data driven (functional unit is not required by the currently executing software and shutting down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache are both interpreted to be data driven, col. 3, lines 47-63).

13. Regarding claim 5, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling/disabling device is adapted to provide a clock to a number of the data processing units which is equal to 0 (all or none of the processing units of Gupta may be enabled or disabled, col. 3, lines 47-51; figures 3-5 and corresponding text).

14. Regarding claim 7, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein each of the processing units is a reconfigurable unit of a multi-dimensional array (each processing unit of Gupta is reconfigurable because it can change its operating mode, col. 3, line 64 through col. 4, line 5).

15. Regarding claim 8, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling disabling device is adapted to selectively enable or disable power supply to the number of data processing units (figure 6 and corresponding text).

16. Regarding claim 9, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling/disabling device is adapted to

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selectively block full clock speed for the number of data processing units (figures 3-5 and corresponding text).

17. Regarding claim 10, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling/disabling device is adapted to be data availability driven (shutting down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache are both interpreted to be data driven, col. 3, lines 47-63; wherein the data availability is interpreted to be available to be placed in an internal cache).

18. Regarding claim 11, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the number of data processing units includes only a single one of the data processing units in the array (Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

19. Regarding claim 12, Gupta teaches a data processing device, comprising:

- a. an array of data processing units (FU_1 - FU_2 , figure 2), the data processing units being connected to at least one of a power supply line (removing power to functional unit, col. 4, lines 5-7; figure 6 and corresponding text) and a clock line (col. 3, line 67 through col. 4, line 5; figures 3-5 and corresponding text); and
- b. an enabling/disabling device (power control 108, figure 2) adapted to, in response to an availability of data for at least one respective one of the data processing units, at least one of:

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i. i) selectively enable or disable power supply to the at least one respective one of the data processing units (removing power to the functional units, col. 4, lines 5-7), and

ii. ii) selectively block full clock speed for the at least one respective one of the data processing units (col. 3, line 67 through col. 4, line 5);

c. wherein the at least one respective one of the data processing units includes less than all of the data processing units in the array (each functional may be provided with its own clock and power control col. 3, lines 47-51; figures 3-6; Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

20. Regarding claim 13, Gupta taught the data processing device according to claim 12, as described above. Gupta further teaches wherein the enabling/disabling device enables the power supply to the respective one of the data processing units only when data is available for the respective one of the data processing units (shutting down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache are both interpreted to be data driven, col. 3, lines 47-63; wherein the data availability is interpreted to be available to be placed in an internal cache; also wherein the software determines that a functional unit is not required by currently executing software, col. 3, lines 44-51).

21. Regarding claim 14, Gupta taught the data processing device according to claim 12, as described above. Gupta further teaches wherein the enabling/disabling device is adapted to make a clock signal available to the respective one of the data processing units only when an operand is ready for the respective one of the data processing units (shutting down an external bus

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interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache are both interpreted to be data driven, col. 3, lines 47-63; block of code sent to a cache are operands).

22. Regarding claim 15, Gupta taught the data processing device according to claim 12, as described above. Gupta further teaches wherein the enabling/disabling device is associated with only a single one of the data processing units (Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

23. Regarding claim 16, Gupta taught the data processing device according to claim 12, as described above. Gupta further teaches wherein the at least one respective one of the data processing units includes only a single one of the data processing units in the array (Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

24. Regarding claim 17, Gupta teaches a processing device, comprising:

a. an array of data processing units (FU_1 - FU_2 , figure 2), the data processing units being connected to at least one of a power supply line (removing power to functional unit, col. 4, lines 5-7; figure 6 and corresponding text) and a clock line (col. 3, line 67 through col. 4, line 5; figures 3-5 and corresponding text); and

b. an enabling/disabling device (power control 108, figure 2) adapted to make a clock signal available to at least one respective one of the data processing units when an operand is ready for the at least one respective one of the data processing units (shutting down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache are both interpreted to be data driven, col.

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3, lines 47-63; wherein the data availability is interpreted to be available to be placed in an internal cache; also wherein the software determines that a functional unit is not required by currently executing software, col. 3, lines 44-51); and

c. wherein the at least one respective one of the data processing units includes less than
5 all of the data processing units in the array (each functional may be provided with its own clock and power control col. 3, lines 47-51; figures 3-6; Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

25. Regarding claim 18, Gupta taught the data processing device according to claim 17, as
10 described above. Gupta further teaches wherein the enabling/disabling device is associated with only a single one of the data processing units (Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

26. Regarding claim 19, Gupta taught the data processing device according to claim 17, as
described above. Gupta further teaches wherein the at least one respective one of the data
15 processing units includes only a single one of the data processing units in the array (Gupta shows that any number of data processing units in the array may be enabled or disabled or have their clock speed controlled, figure 2).

Response to Arguments

20 27. Applicant's arguments filed 12/18/06 have been fully considered but they are not persuasive.

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28. Applicant argues in substance neither Durham nor Gupta teach that an enabling/disabling device is data driven. The examiner respectfully disagrees.

29. Regarding Durham, applicant is directed to col. 4, lines 45-54 of Durham. Durham measures values of power then places a functional unit in power mode based on the

5 measurement. The measurements are data, thus the enabling/disabling device of Durham are data driven.

30. Regarding Gupta, applicant further asserts that Gupta device is driven by instructions rather than by data. The examiner contends that a device being driven by instruction is inherently driven by data from those instructions. Instructions are portions of software that

10 contain data. Gupta uses software to control power to a functional unit. The software generates values based on software being executed by the processing device, as shown at col. 3, lines 47-

62. Software being currently executed inherently contains data that determines which functional unit is required. Also, Gupta refers to blocks of code that are determined to fit in an internal cache would constitute data, that is used to shut down a functional unit. Gupta merely uses

15 software rather than hardware to determine which functional units to shut down. The software of Gupta inherently requires data. Thus, the device of Gupta is driven by data.

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Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

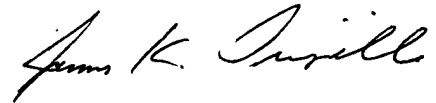
A shortened statutory period for reply to this final action is set to expire THREE
5 MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37
CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,
10 however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

15 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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